AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph at page 15, line 29 to page 16, line 8 with the following amended paragraph:

Thus, in the example, to determine the feasibility of merging the flow set having the flows a, b and c with the flow set having the flows d, e and f only the greater bandwidth of the two flow sets needs to be accommodated by an interconnect device. Because each of these flow sets has a bandwidth requirement of 99 Mb/s, the greater of the two is also 99 Mb/s. Because this requirement is less than the maximum bandwidth capacity of the available interconnect devices, this means that these two flow sets can be merged to alleviate the port violations remaining at the terminal nodes 50-54. This is shown in Figure [[10]]11, where the device 164 merges the flow set having the flow of a, the flow of b and the flow of c with the flow set having the flow of d, the flow of e and the flow of f. In addition, the device 166 is eliminated.

Please replace the paragraph at page 16, line 19 to page 17, line 8 with the following amended paragraph:

Under certain circumstances, a single-layer fabric may not eliminate all of the port violations. In which case, the methods 200 and 300, by themselves may not result in a fabric design in which there are no port violations. Thus, in one embodiment, the present invention may address remaining port violations by recursively generating one or more additional layers of interconnect fabric nodes. For port violations at source nodes, the problem (i.e. the current fabric configuration and the applicable design information) may be recast such that the device nodes are treated as the terminal nodes. Then, one or more additional layers of device nodes may be inserted between the source nodes and the device nodes to relieve the port violations at source nodes. This results in links between device nodes and, thus, increases the number of layers in the interconnect fabric. Similarly, for terminal port violations, the problem may be recast such that the device nodes are treated as the source nodes. Then, one or more additional layers of device nodes may be inserted in between the device nodes and the terminal nodes to relieve the terminal node port

violations. This also results in links between the device nodes and, thus, increases the number of layers in the interconnect fabric. Such a technique is disclosed in co-pending U.S. Application No. [[_____]]10/027,564, entitled, "Designing Interconnect Fabrics," and filed December 19, 2001, the contents of which are hereby incorporated by reference and which is continuation-in-part of U.S. Application No. 09/707,227, filed November 16, 2000.